CLAIMS:

1. A method of making a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer; said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating polymer; characterised in that said method comprises the steps of:

(i) depositing on the first electrode a layer of a solution containing material for forming the semiconductive layer and material for forming the dielectric layer; and

(ii) optionally curing the layer deposited in step (i);

wherein, in step (i), the solvent drying time, the temperature of the first electrode and the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self-organisation to form an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer.

2. A method according to claim 1, wherein the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) is in the range of from 0.5 to 2.

3. A method according to claim 1 or claim 2, wherein the solvent drying time is in the range of from 0.1 to 100s.

4. A method according to any one of the preceding claims, wherein the material for forming the dielectric layer is mixed with the material for forming the semiconductive layer in the solution.

5. A method according to claim 4, wherein the material for forming the dielectric layer comprises oligomers and/or monomers for forming the insulating polymer and the material for forming the semiconductive layer comprises a semiconductive polymer and/or oligomers for forming the semiconductive polymer.

6. A method according to claim 4, wherein the material for forming the dielectric layer comprises an insulating polymer and the material for forming the semiconductive layer comprises a semiconductive polymer and/or oligomers for forming the semiconductive polymer.

7. A method according to any one of claims 1 to 3, wherein the material for forming the semiconductive layer and the material for forming the dielectric layer comprises a diblock polymer, said polymer comprising a semiconductive block for forming the semiconductive layer and a dielectric block for forming the dielectric layer.

8. A method according to any one of the preceding claims, wherein the material for forming the semiconductive layer comprises one or more aromatic or heteroaromatic structural units.

9. A method according to claim 8, wherein the one or more aromatic or heteroaromatic units independently are selected from the group consisting of fluorenedyil, phenylene, phenylene vinylene, triarylamine, thiophenediyl, thiophene, oxadiazole and benzothiadiazole.

10. A method according to any one of the preceding claims, wherein the material for forming the dielectric layer comprises crosslinkable groups.

11. A method according to any one of the preceding claims, wherein the material for forming the dielectric layer comprises one or more units having a low cohesive-energy density.

12. A method according to claim 11, wherein the one or more units having a low cohesive-energy density are selected from the group consisting of siloxane, perfluoroalkyl, perfluoroarylene ether, perfluoroalkylene ether.

13. A method according to claim 11 or claim 12, wherein the material for forming the dielectric layer has a surface tension in the range of from 15 to 35 dyn/cm.

14. A method according to any one of the preceding claims, wherein the transistor is in top-gate configuration.

15. A method according to any one of claims 1 to 13, wherein the transistor is in bottom-gate configuration.

16. A method according to claim 15, wherein the material for forming the dielectric layer comprises one or more units having high affinity for the first electrode.

17. A method according to claim 15, wherein the first electrode is surface treated prior to step (i) with a material containing one or more units having high affinity for the first electrode.

18. A method according to any one of the preceding claims, wherein the thickness of the dielectric layer is below 400nm.

19. A method according to any one of the preceding claims, wherein the thickness of the semiconductive layer is in the range of 10nm to 300nm.

20. A method according to any one of the preceding claims, wherein the transistor is a field-effect transistor.

21. A method according to any one of claims 1 to 19, wherein the transistor is a phototransistor.

22. A transistor obtainable by the method as defined in any one of claims 1 to 21.

23. A method of making an electronic or optoelectronic device comprising a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer; said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating

polymer; characterised in that said method comprises the steps of:

(i) depositing on the first electrode a layer of a solution containing material for forming the semiconductive layer and material for forming the dielectric layer; and

(ii) optionally curing the layer deposited in step (i);

wherein the solvent drying time, the temperature of the first electrode and the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self-organisation to form an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer.

24. A method according to claim 23, wherein the electronic or optoelectronic device comprises an RF tag, electronic paper, chemical sensor, logic circuit, amplifier, or driver circuit.

25. An electronic or optoelectronic device obtainable by the method as defined in claim 23 or claim 24.

26. Apparatus for controlling solvent drying time during deposition of a solution containing material for forming one or two polymer layers on a substrate in an electronic or optoelectronic device, said apparatus comprising a plate for carrying the substrate; characterised in that the plate is

positioned inside an enclosure, said enclosure having a solvent vapour inlet port and an outlet port.

27. Apparatus according to claim 26, wherein said apparatus has means for controlling the temperature of the substrate.

28. Apparatus according to claim 26 or 27, wherein a grid for maintaining even gas flow is positioned inside the enclosure.

29. Use of apparatus as defined in any one of claims 26 to 28 in a method for making a transistor.

30. Use according to claim 29, wherein the transistor is a field-effect transistor.

31. Use according to claim 29, wherein the transistor is a phototransistor.

32. Use of apparatus as defined in any one of claims 26 to 28 in a method for making an electronic or optoelectronic device.

33. Use according to claim 32, wherein the electronic or optoelectronic device comprises an RF tag, electronic paper, chemical sensor, logic circuit, amplifier, or driver circuit.